

Schematics Version History Table :

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3.1B	3.1B	32		06/02/ ' 06
3.1C	3.1C	32		06/28/ ' 06
3.1D	3.1D	32		07/02/ ' 06

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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	16	C/D/E/F	PREQ-1	PGNT-1
PCI2	17	D/E/F/G	PREQ-2	PGNT-2
PCI3	18	E/F/G/H	PREQ-3	PGNT-3
LAN	25	F	PREQ-4	PGNT-4

VRM
ISL6566CR

ICS952647
48pin SSOP

intel
P4 Processor
775 pin

re.2.0 Prescott, Cedar Mill & Smithfield

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz

BW : 1.066GB/s @ Freq : 66MHz
AGP1 Slot 132p
8X / 1.5V
VGA (G only)

intel
iSP/G
932pin FC-BGA

BW : 2.1GB/s @ DDR : 200/266/333MHz & Freq : 133MHz
BW : 3.2GB/s @ DDR : 266/333/400MHz & Freq : 200MHz

DDIMM1: DDR Socket 184P
DDIMM2 : DDR Socket 184P

USB V2.0
USB1 2 ports
USB2 2 ports
USB3 2 ports
USB4 2 ports
USBLAN 8 ports
IDE2 40pin
IDE1 40pin

Up to Ultra ATA/100
Two IDE Channel

intel
ICH5
460pin EBGA

BW : 133MB/s @ Freq : 33MHz

SATA1 7Pin
SATA2 7pin

PCI1 Slot 120pin @ AD16
PCI2 Slot 120pin @ AD17
PCI3 Slot 120pin @ AD18

Audio Codec
ALC655

AC'97 & Lan I/F

intel
FWH
32pin PLCC

LPC bus

Super I/O
W83627EHF
128pin PQFP

Lan Chip
RTL8100C
100pin

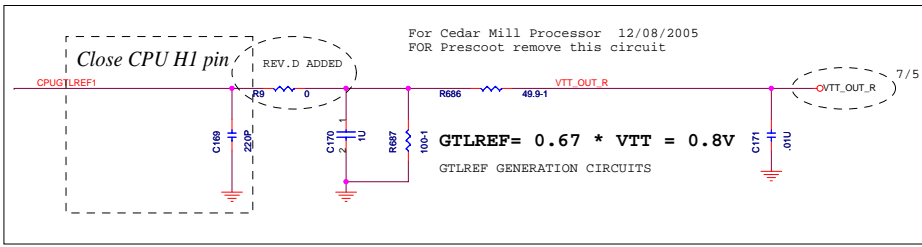
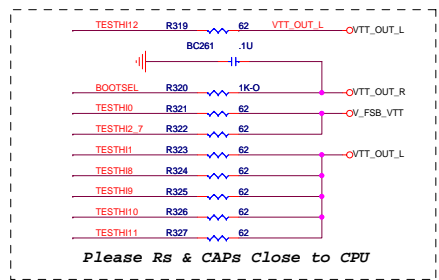
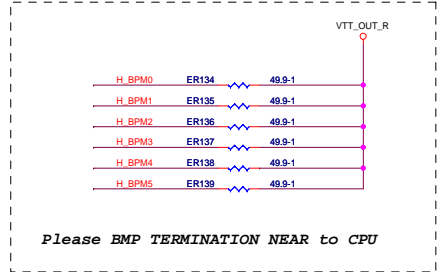
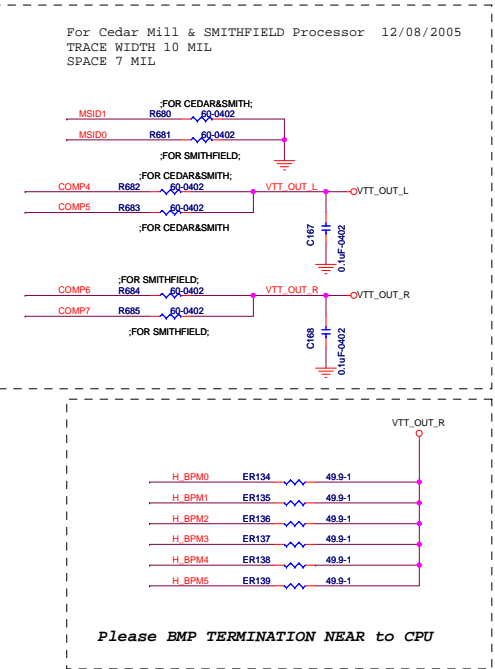
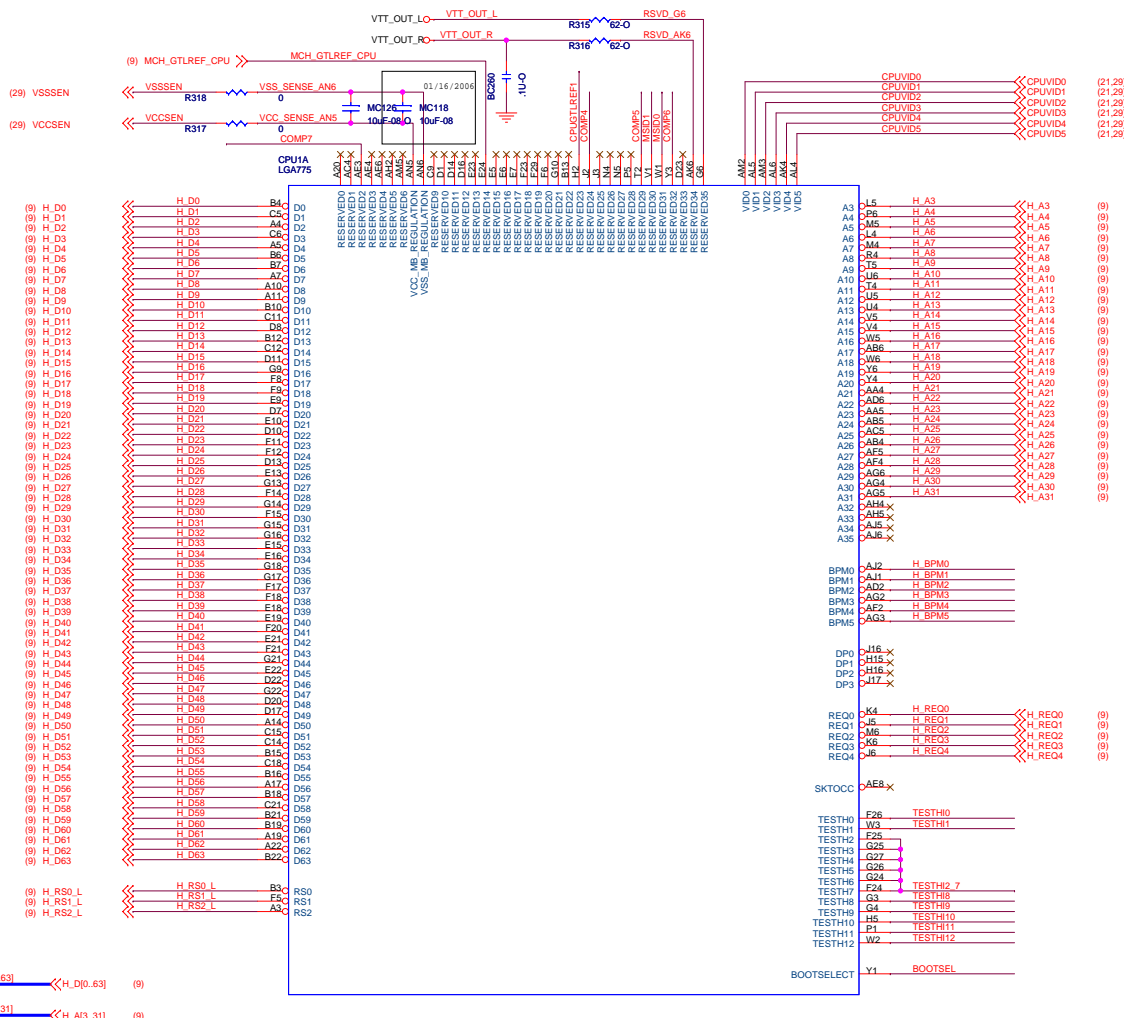
USBLAN
RJ45

Mic In
Line Out
Line In

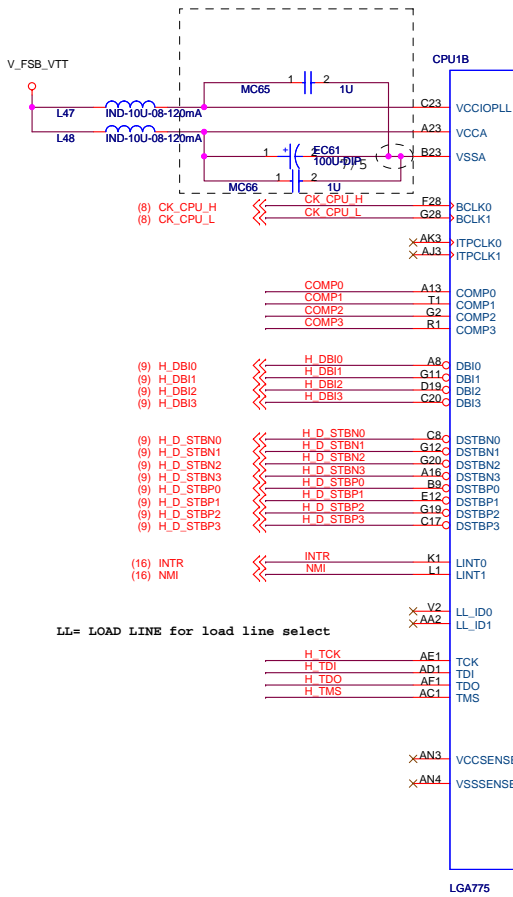


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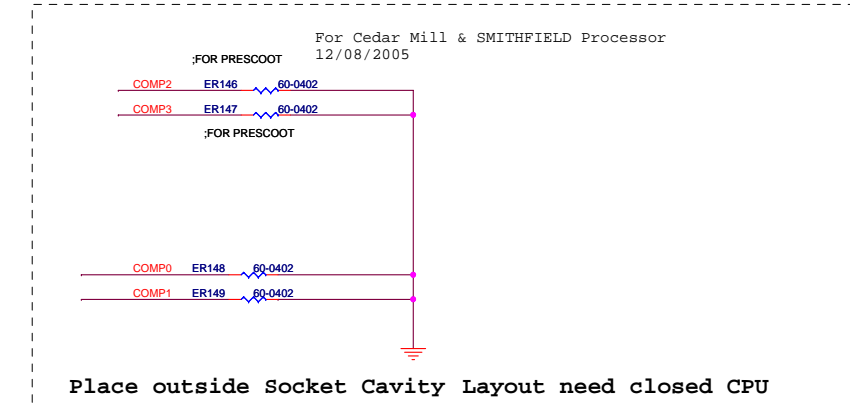
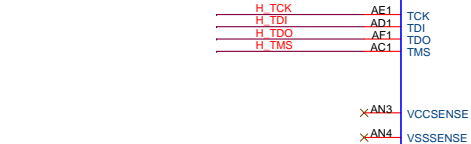
Title System Block Diagram		
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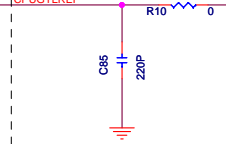
Place componets as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils



LL= LOAD LINE for load line select

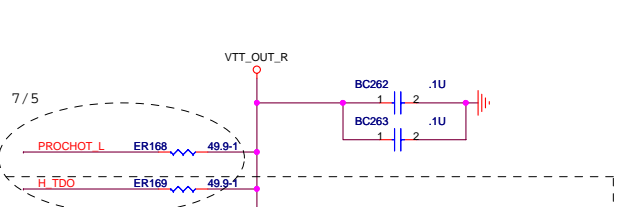
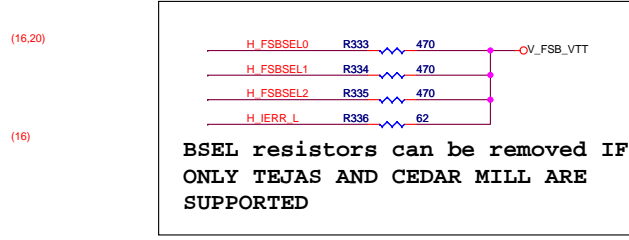
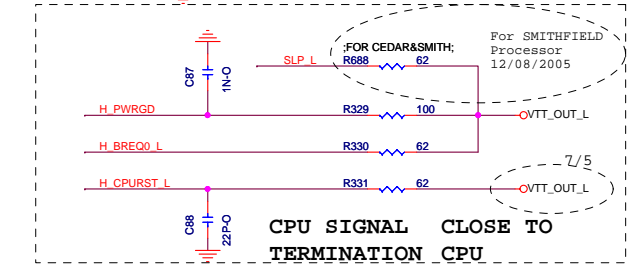
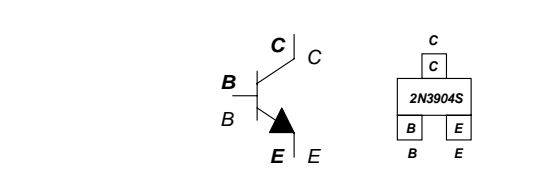
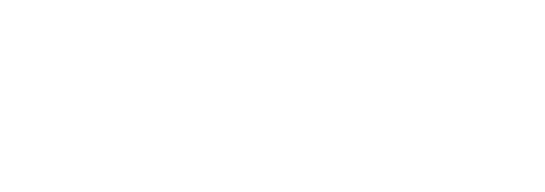
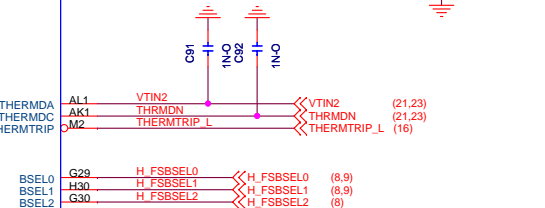
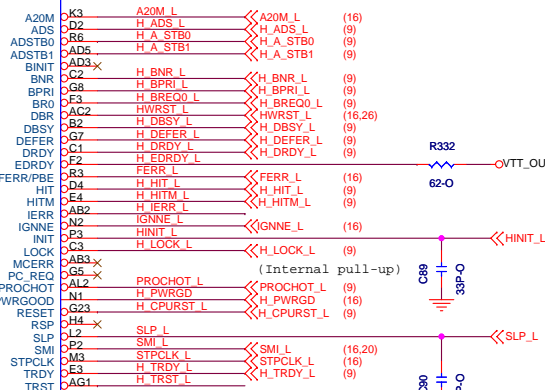


Close CPU H1 pin



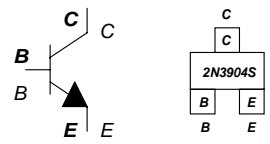
GTLREF = 0.67 * VTT = 0.8V

GTLREF GENERATION CIRCUITS



PLACE TCK/TDI/TMS TERMINATION NEAR CPU
WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.

PLACE TRST_L TERMINATION ANYWHERE ON ROUTE



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P4 LGA775P Part B

865GV-M8

Rev 3.1D

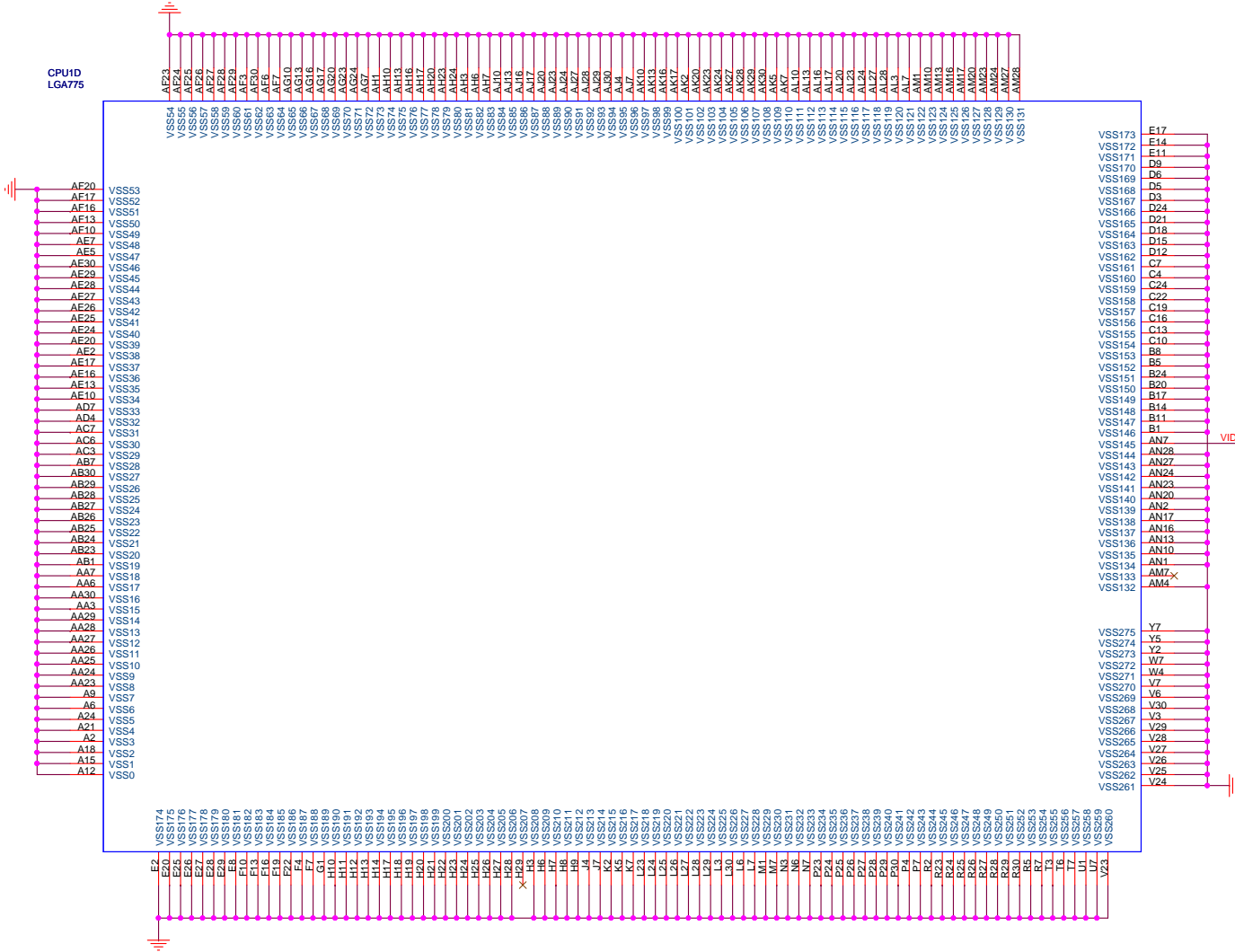
Date: Friday, July 07, 2006

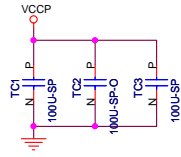
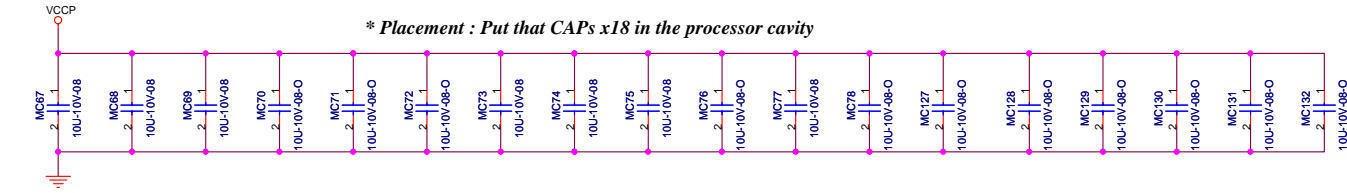
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CPU1C
LGA775

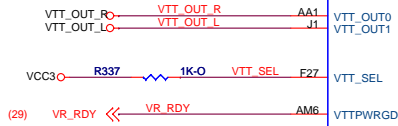
CPU1D
LGA775



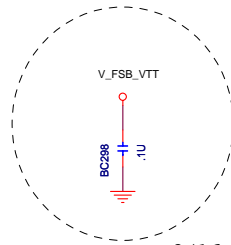
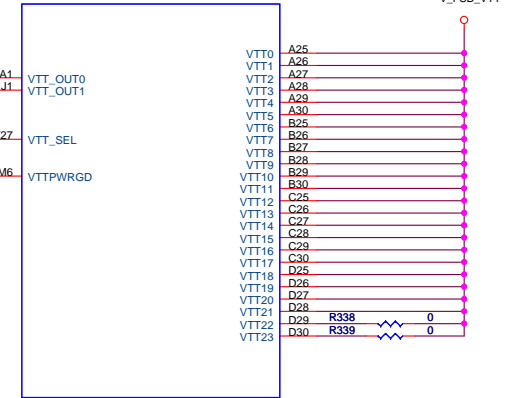


MC109,MC110 near to pin V26 & U27

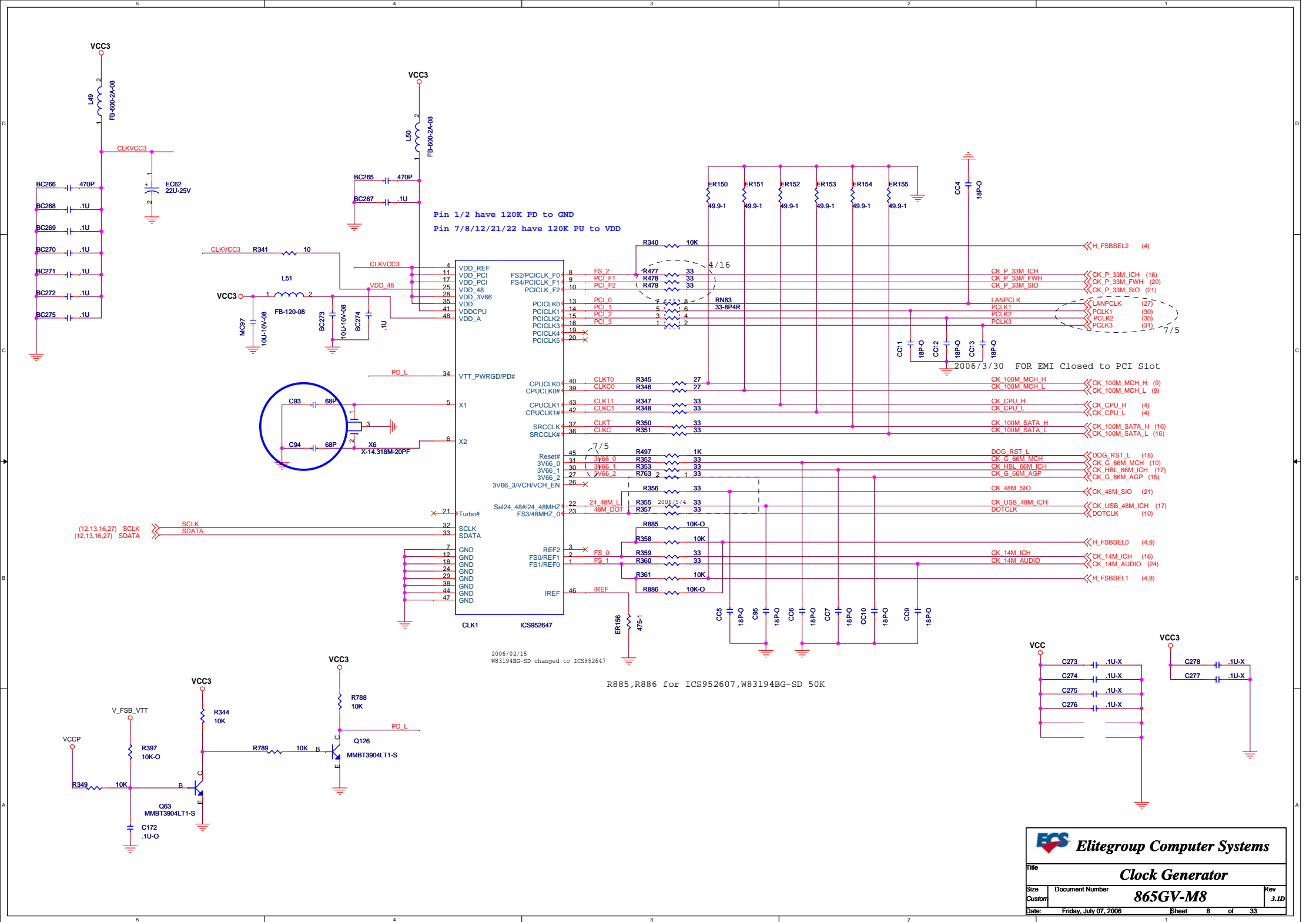
VTT_SEL=0 for the Tejas processor

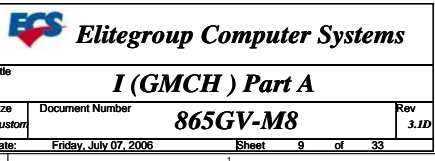
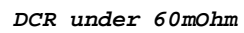
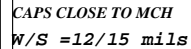
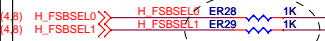


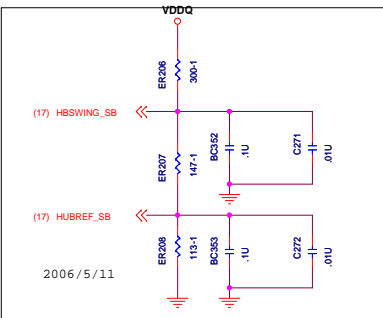
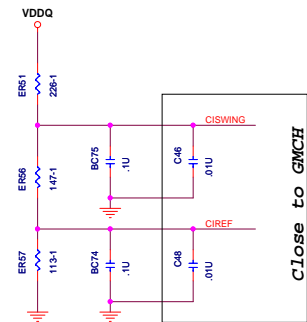
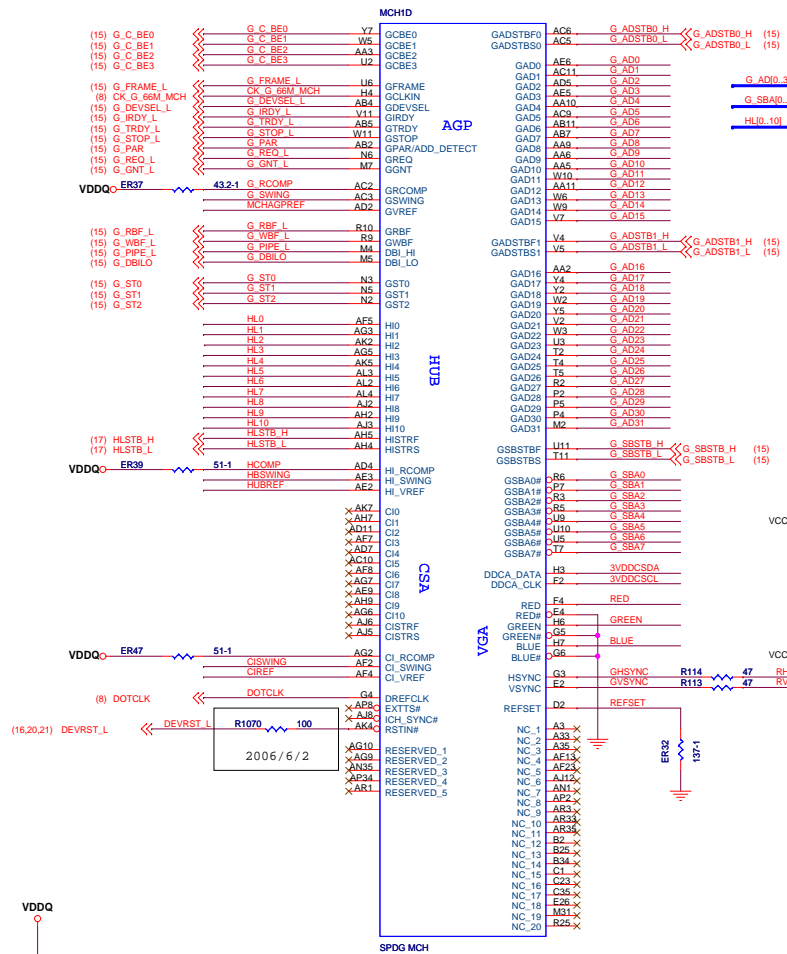
CPU1E
LGA775



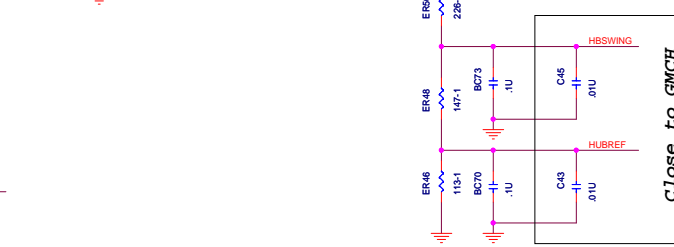
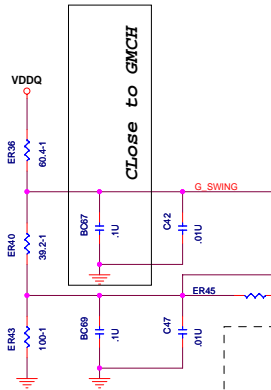
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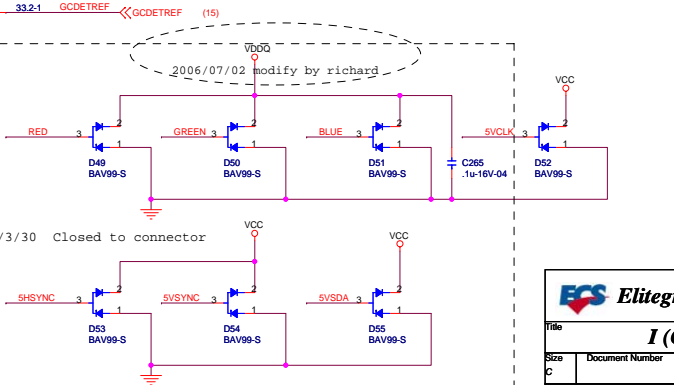


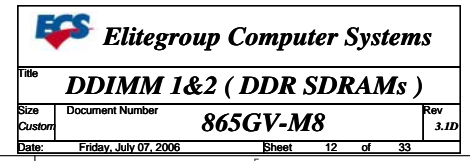
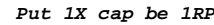
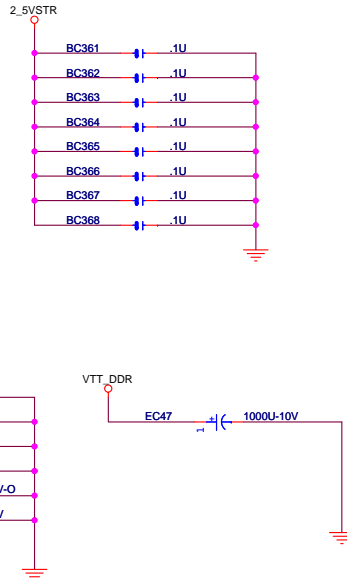


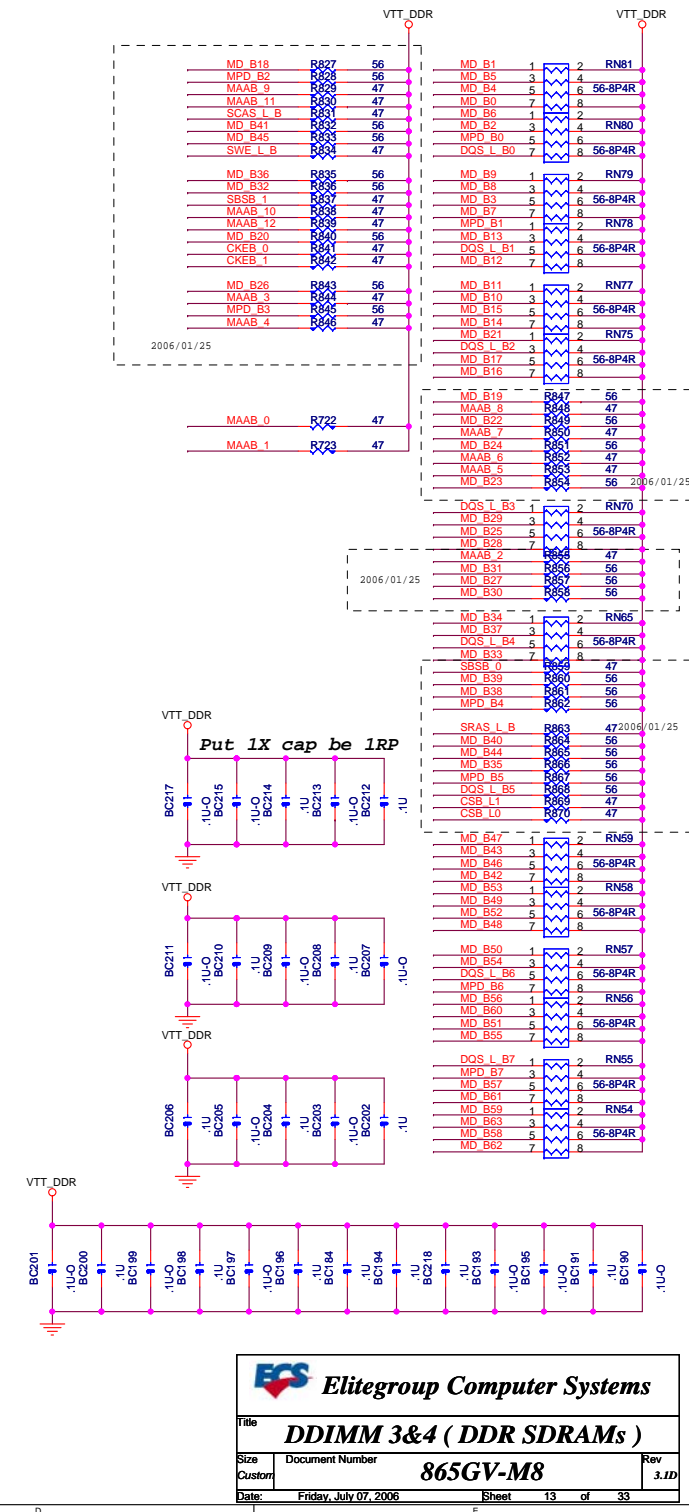
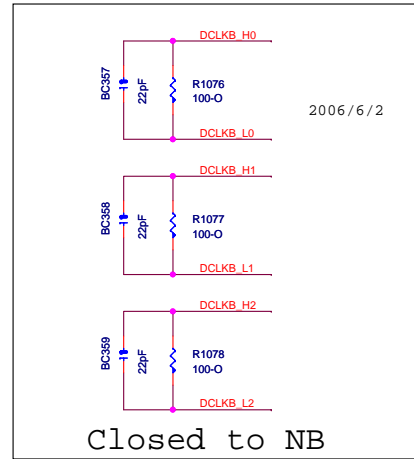
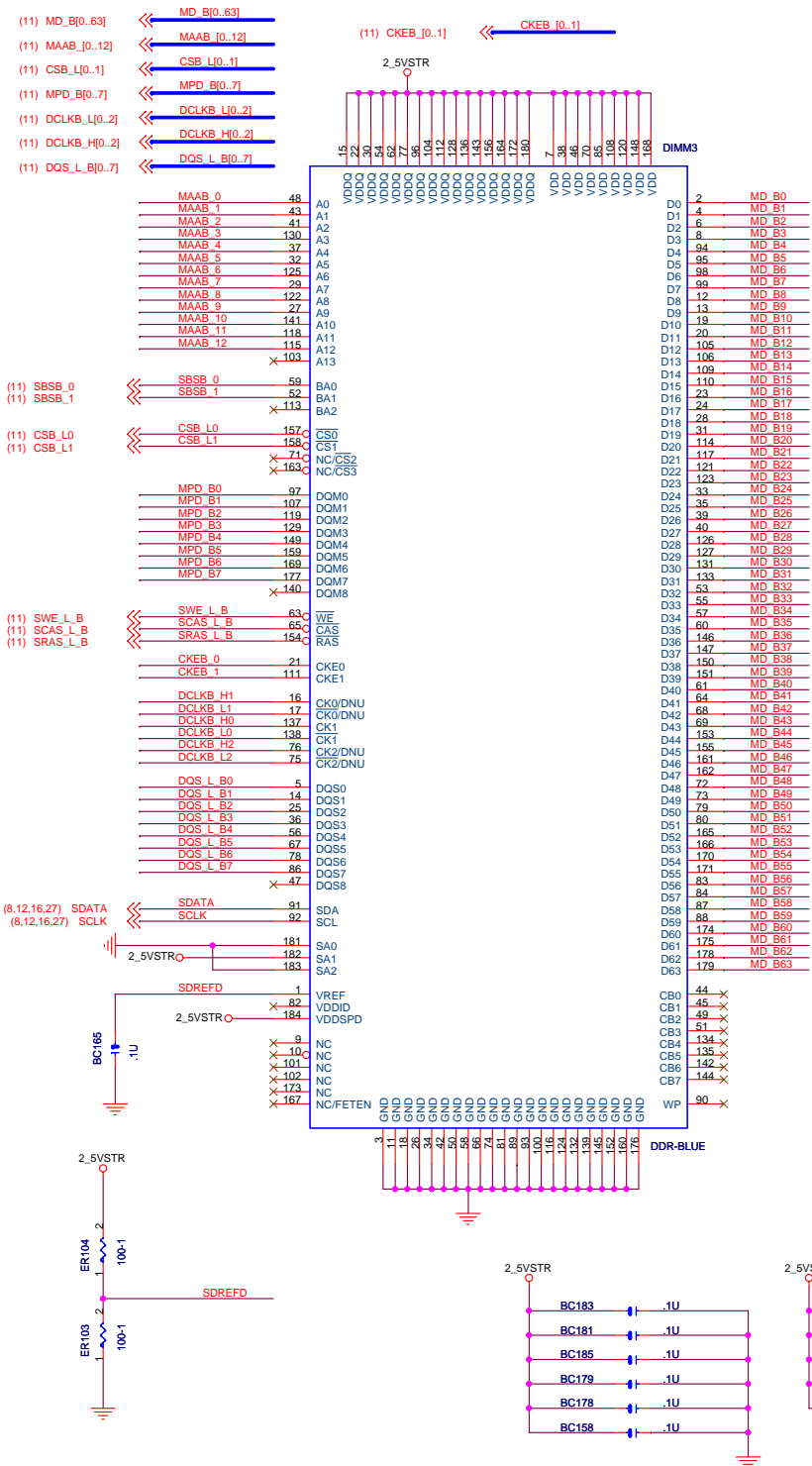
7/15

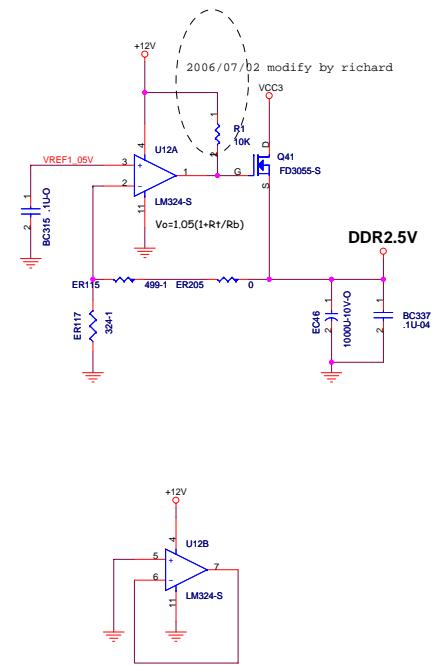
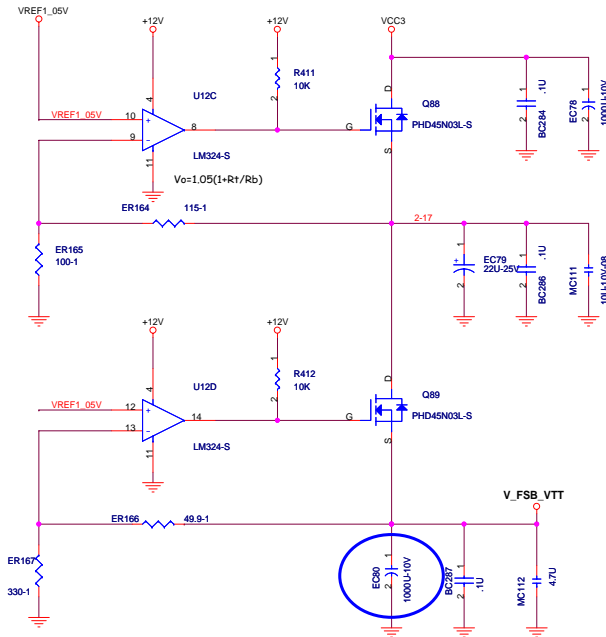
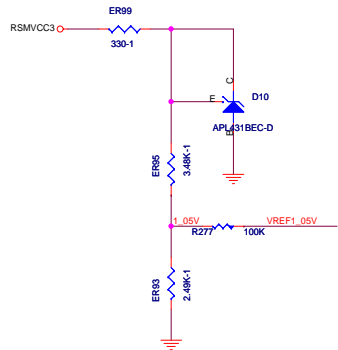
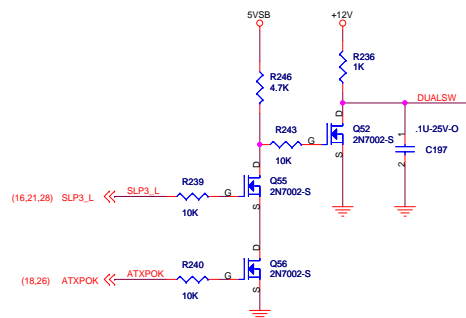
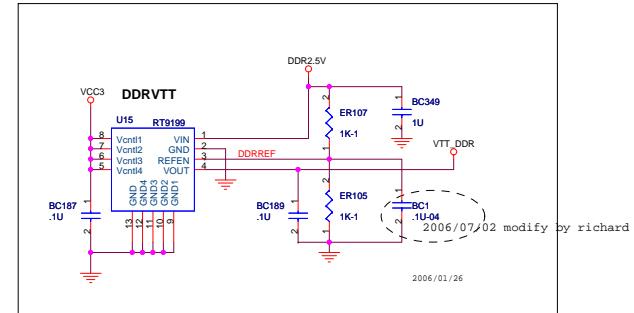
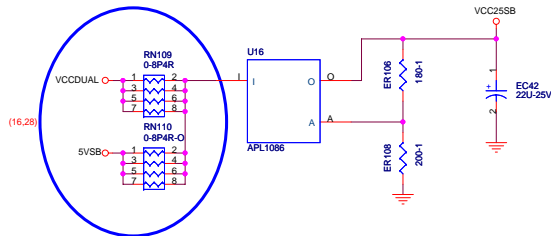
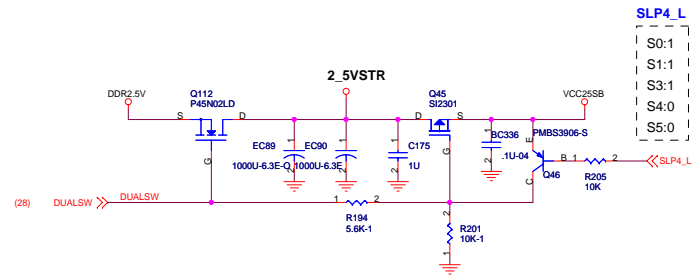


Divider place middle between GMCH and ICH5









(10) G_AD[0..31] << G_AD[0..31]
(10) G_SBA[0..7] << G_SBA[0..7]
(10) G_C_BE0 << G_C_BE0
(10) G_C_BE1 << G_C_BE1
(10) G_C_BE2 << G_C_BE2
(10) G_C_BE3 << G_C_BE3

(10) G_FRAME_L << G_FRAME_L
(10) G_DEVSEL_L << G_DEVSEL_L
(10) G_IRDY_L << G_IRDY_L
(10) G_TRDY_L << G_TRDY_L
(10) G_STOP_L << G_STOP_L
(10) G_PAR << G_PAR
(10) G_REQ_L << G_REQ_L
(10) G_GNT_L << G_GNT_L
(10) G_PIPE_L << G_PIPE_L

(10) G_ADSTB0_H << G_ADSTB0_H
(10) G_ADSTB0_L << G_ADSTB0_L
(10) G_ADSTB1_H << G_ADSTB1_H
(10) G_ADSTB1_L << G_ADSTB1_L
(10) G_SBSTB_H << G_SBSTB_H
(10) G_SBSTB_L << G_SBSTB_L

G_SERR_R_L << R133 6.8K << VDDQ

(10) G_ST0 << G_ST0
(10) G_ST1 << G_ST1
(10) G_ST2 << G_ST2

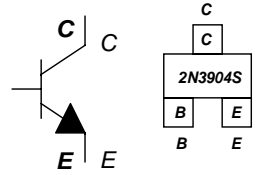
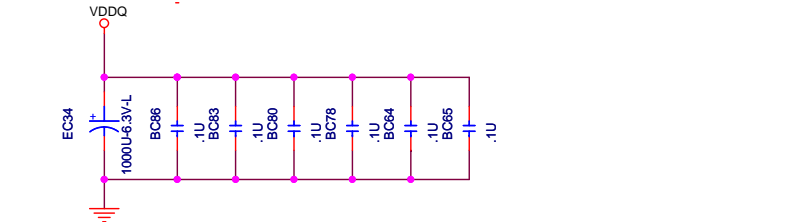
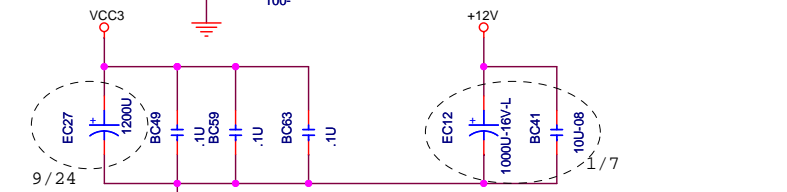
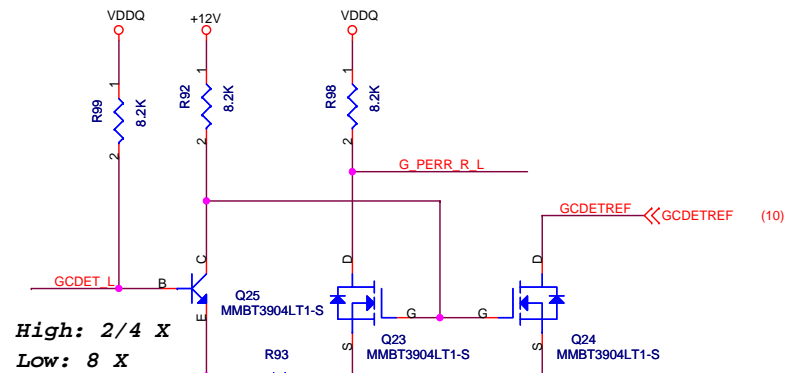
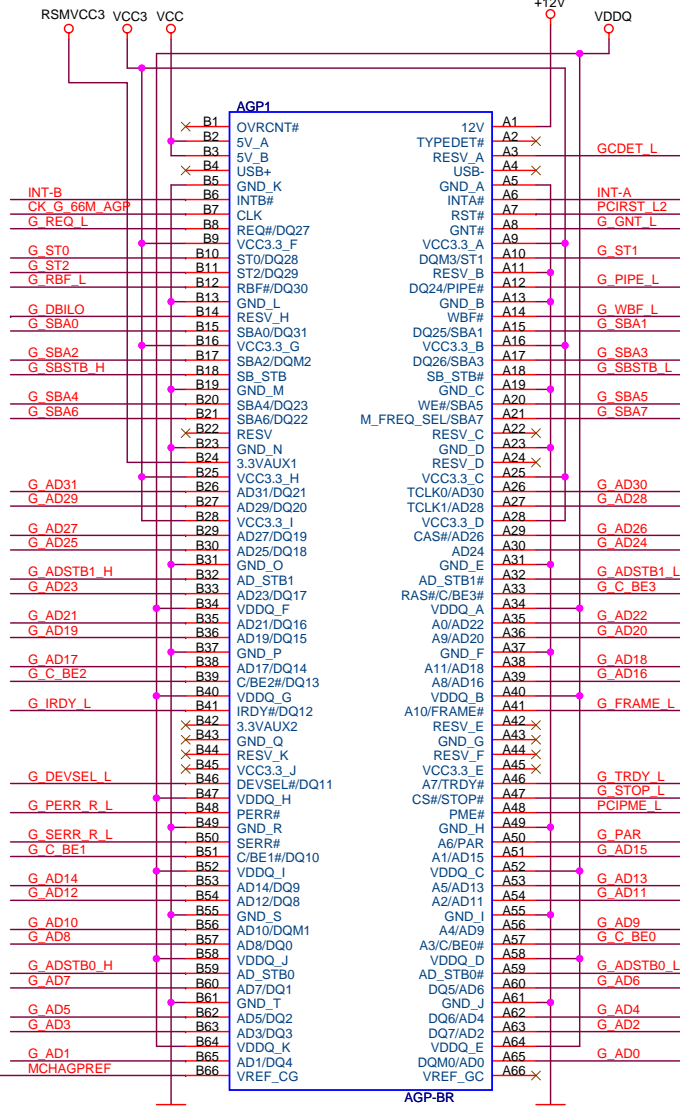
(10) G_DBILO << G_DBILO
(10) G_RBF_L << G_RBF_L
(10) G_WBF_L << G_WBF_L

(8) CK_G_66M_AGP << CK_G_66M_AGP

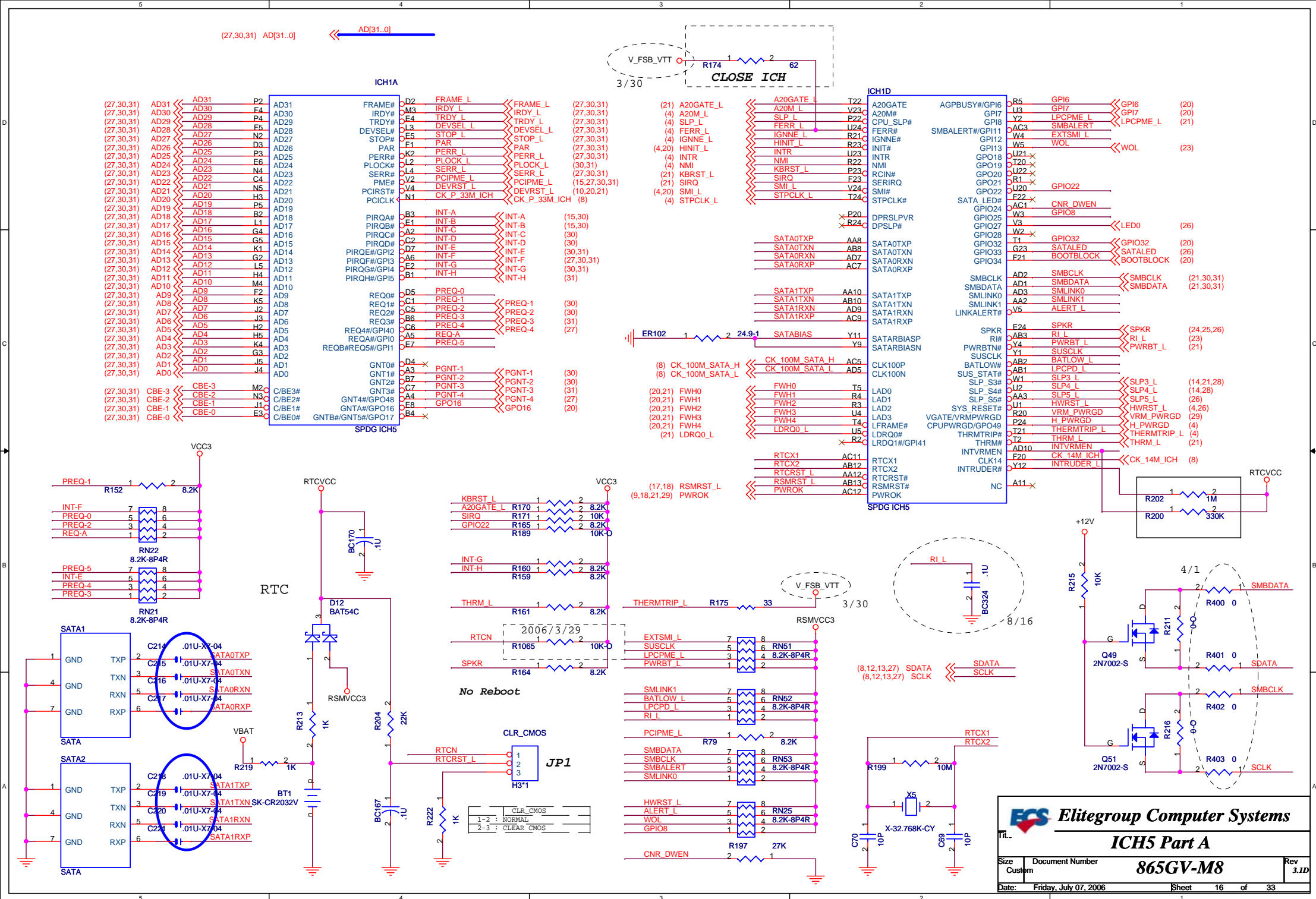
(16,30) INT-A << INT-A
(16,30) INT-B << INT-B

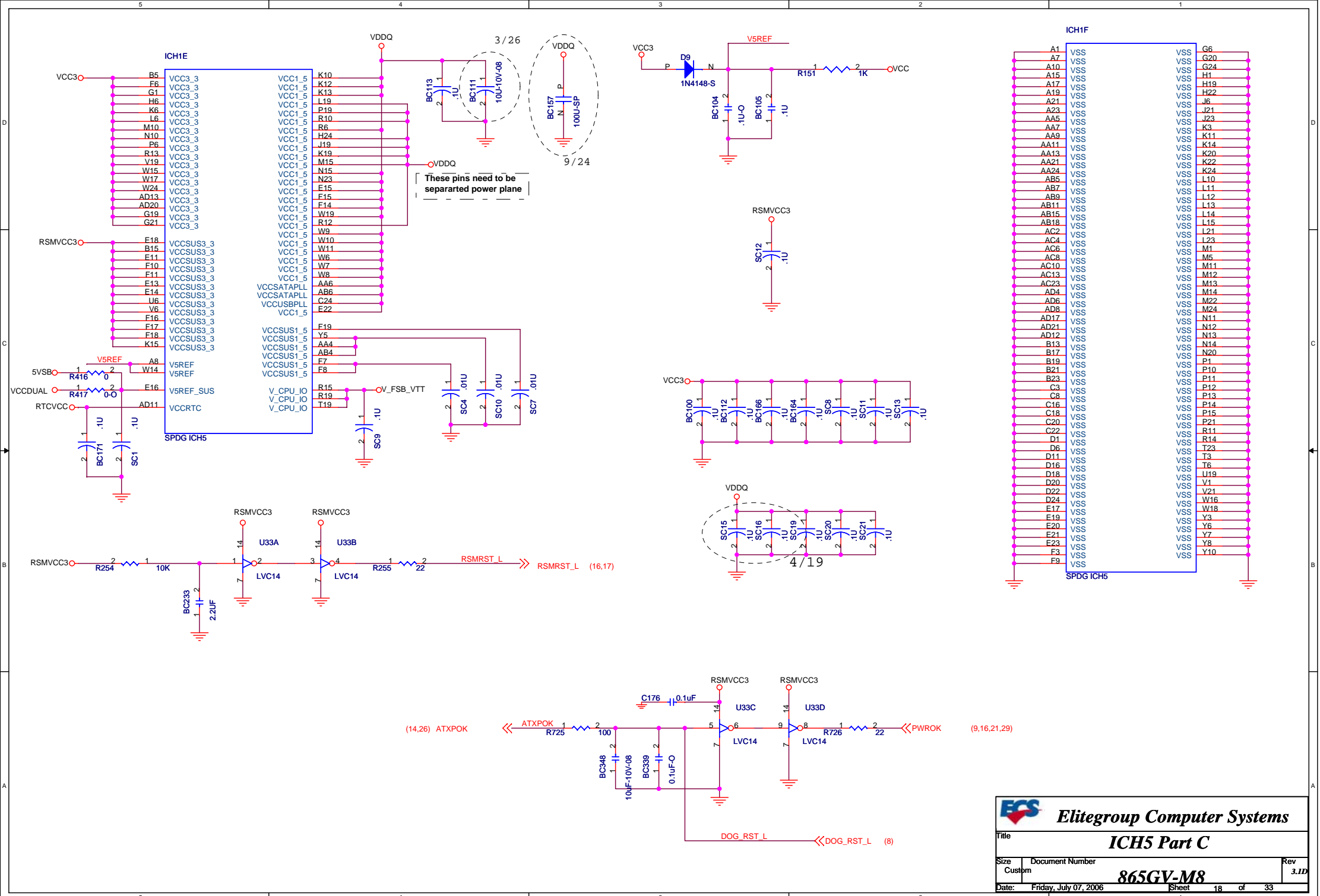
(20,21,30,31) PCIRST_L2 << PCIRST_L2

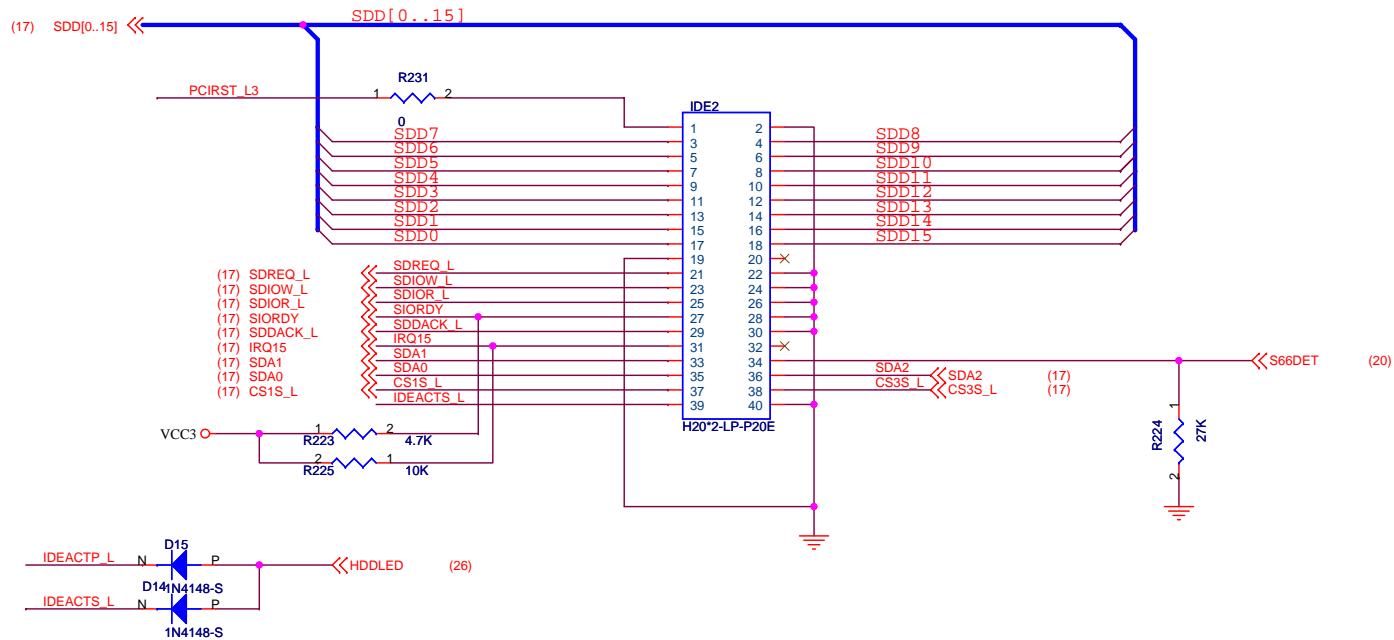
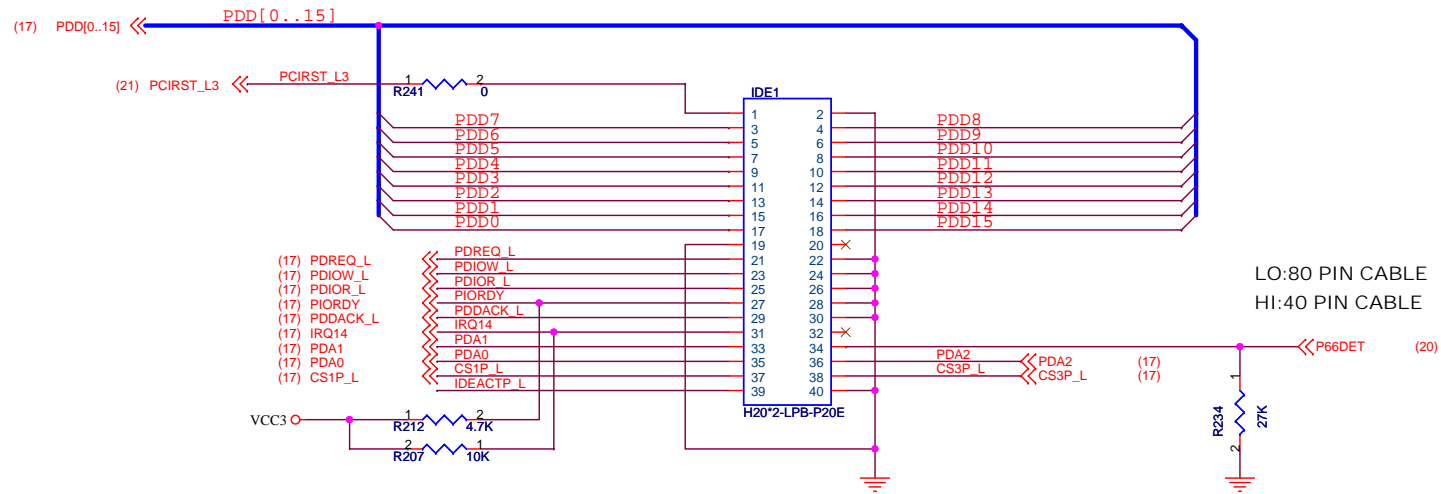
(16,27,30,31) PCIPME_L << PCIPME_L




Elitegroup Computer Systems		
AGP Express		
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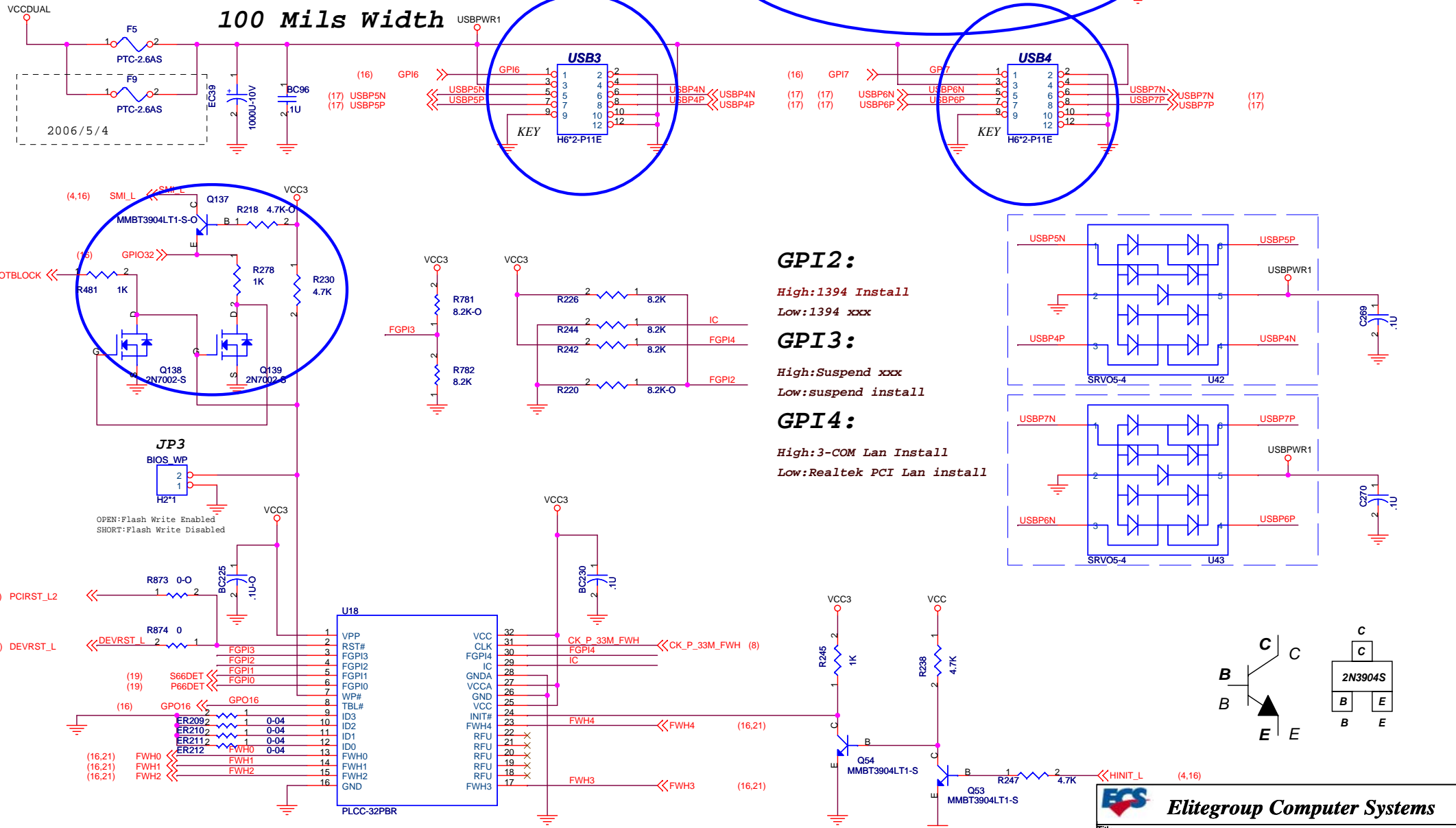


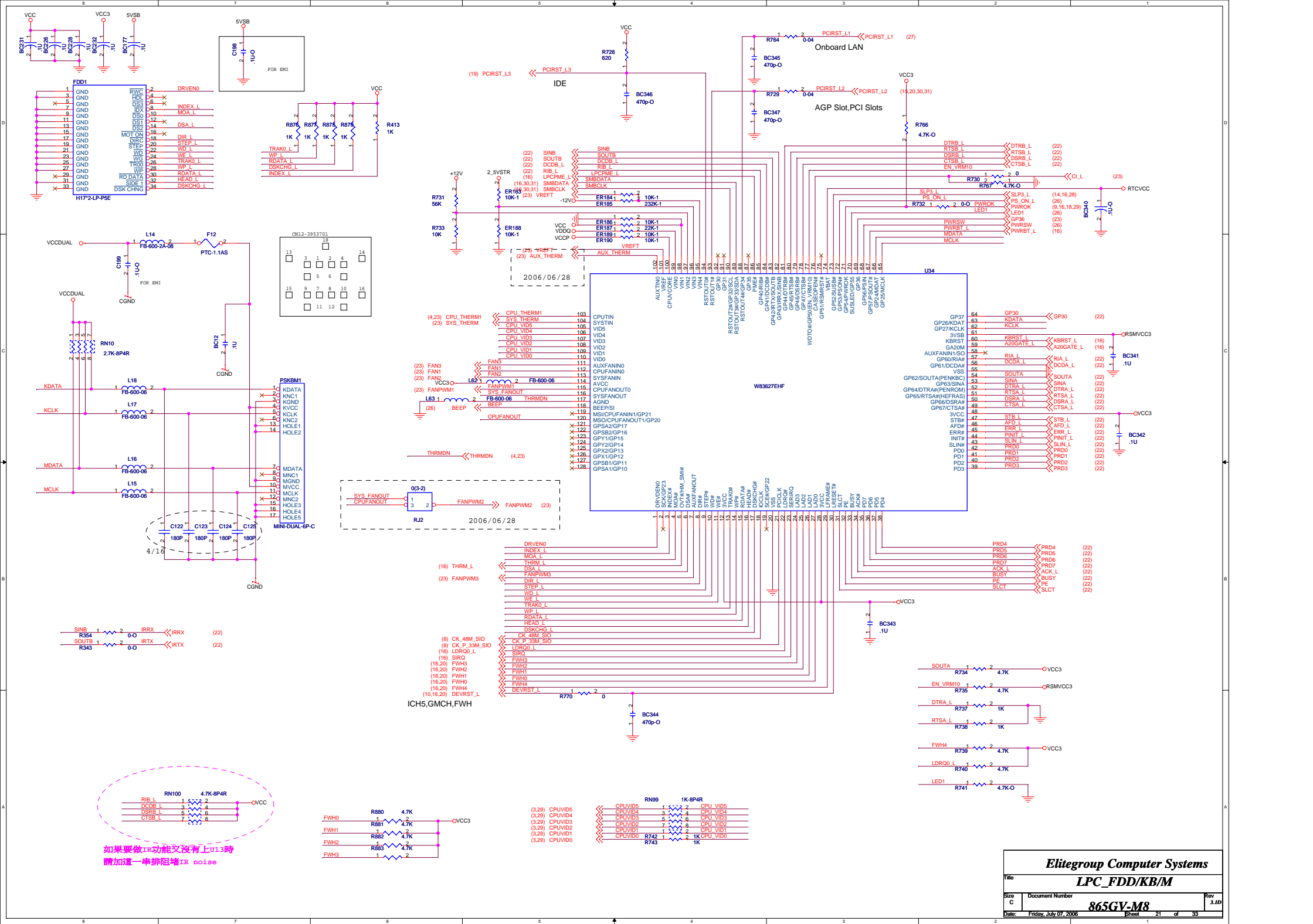


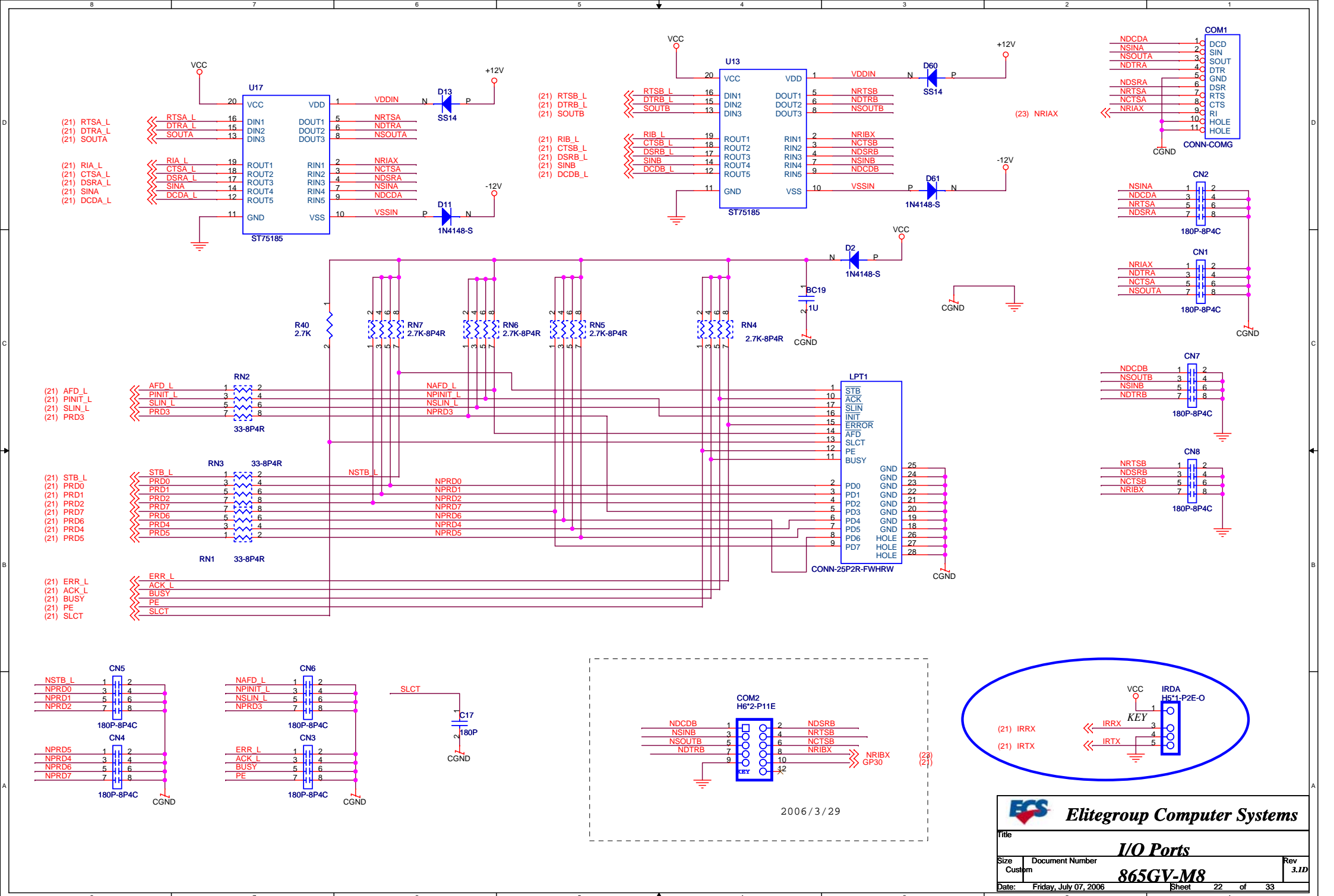
MAX TRACE LENGTH IS 8"

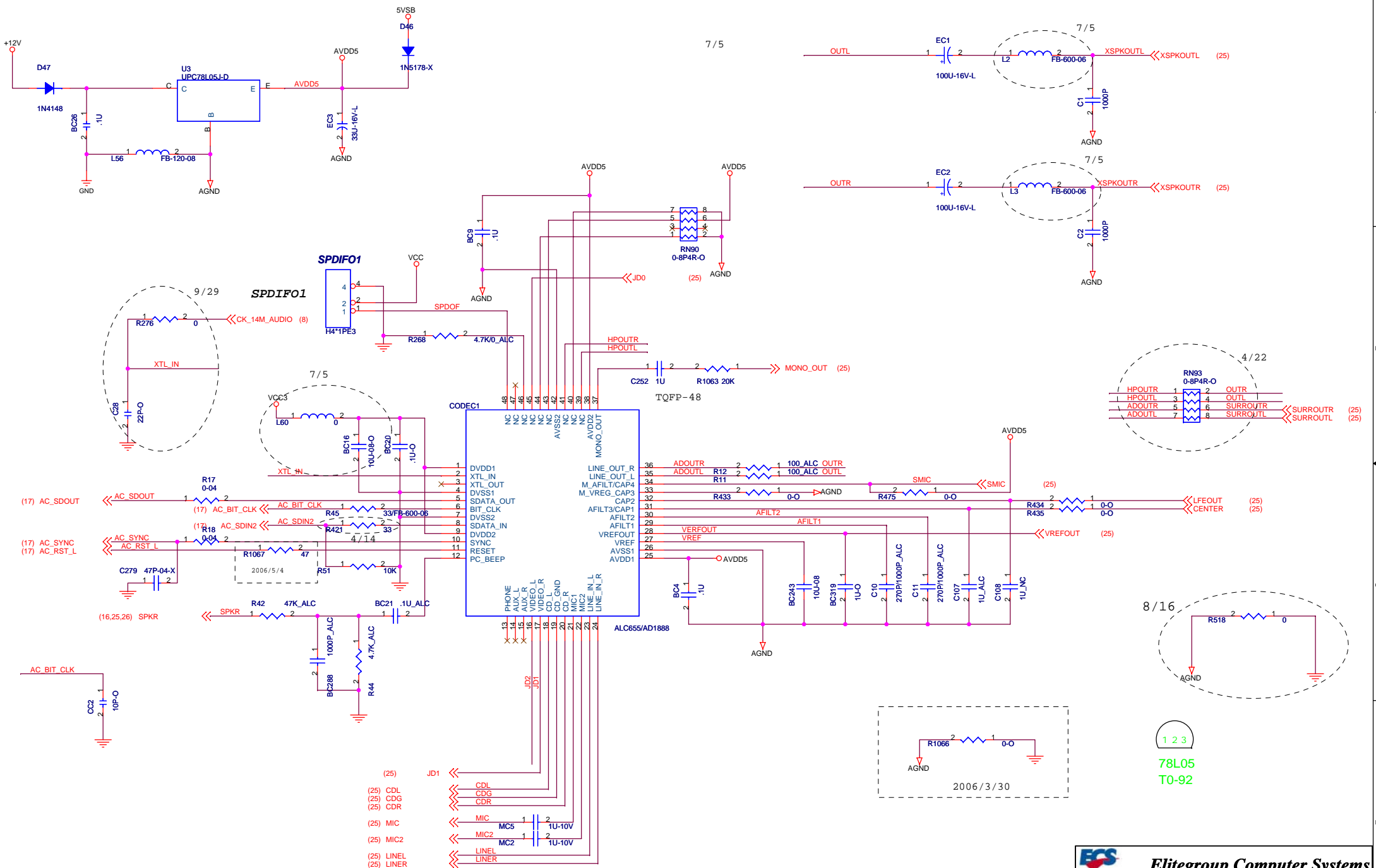
 Elitegroup Computer Systems		
IDE Connector		
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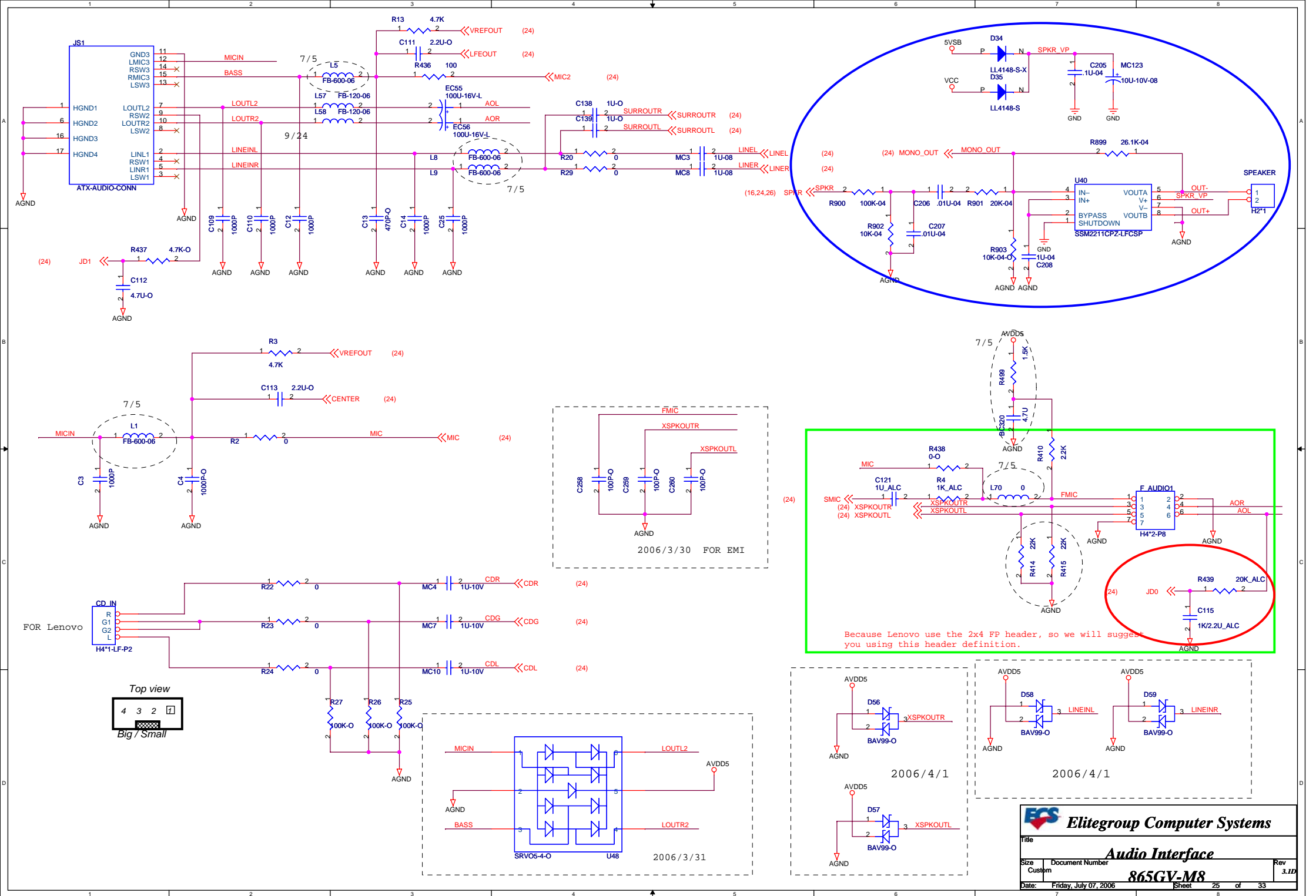
USB PORT INTERFACE

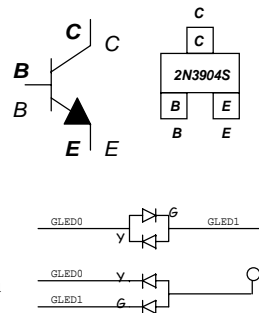
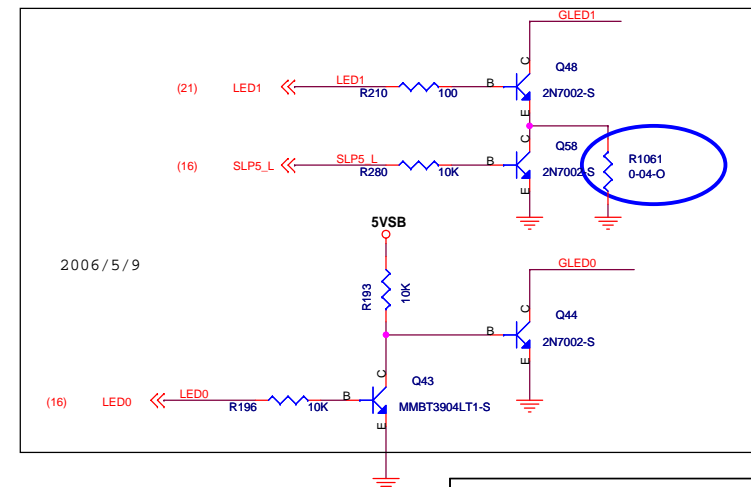
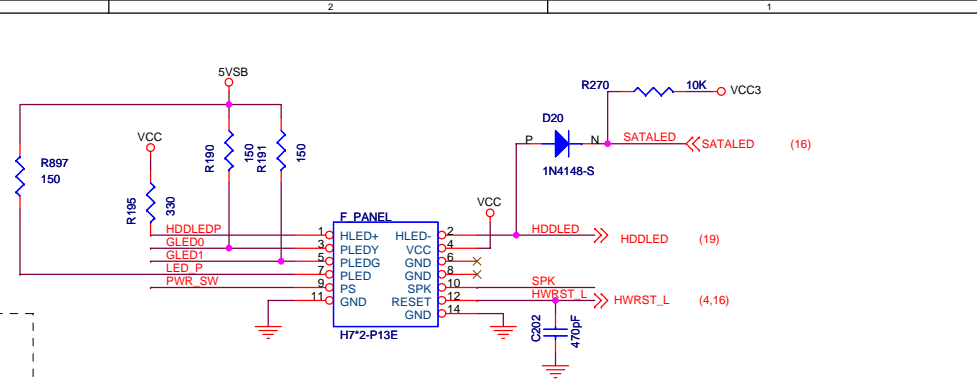





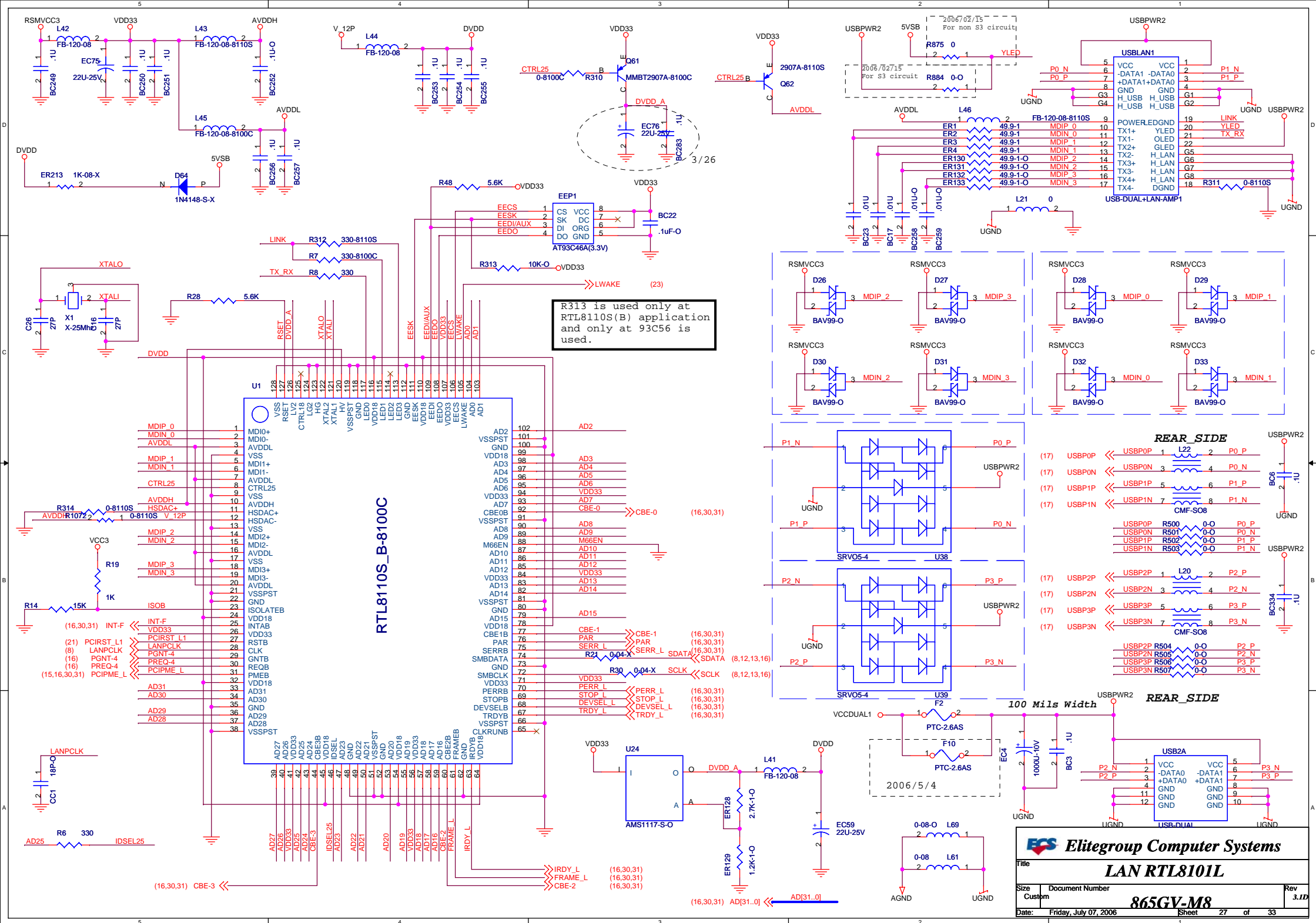


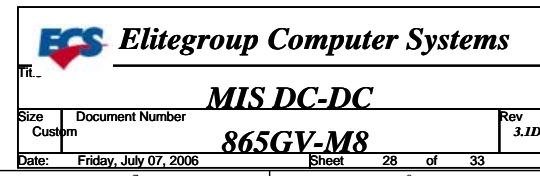
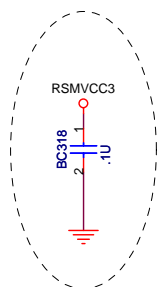


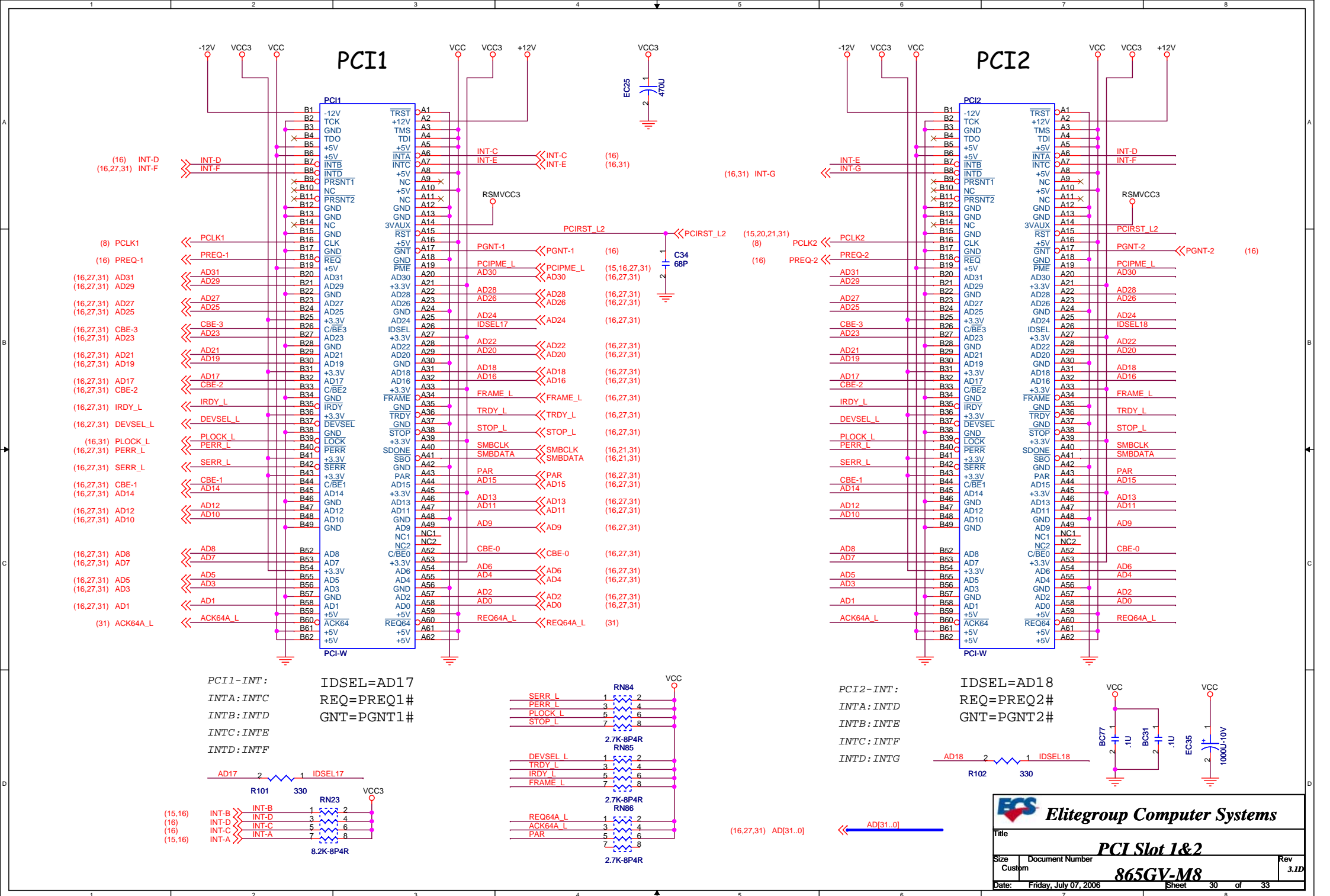


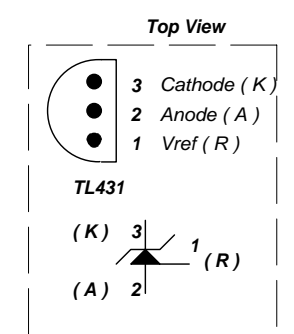
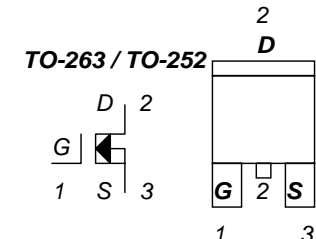
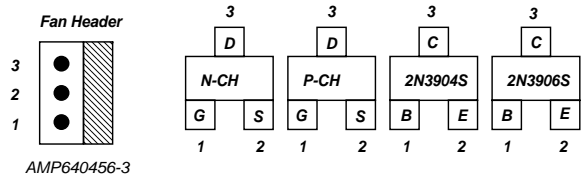
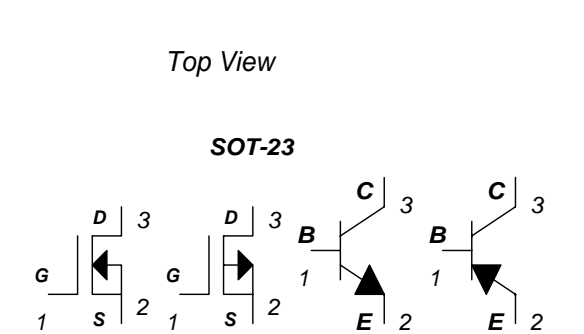
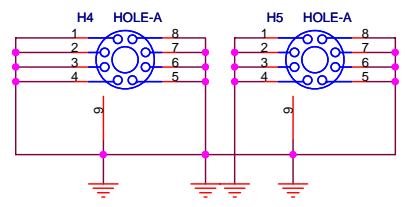
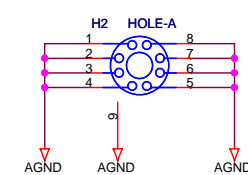
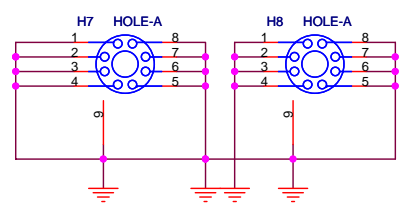
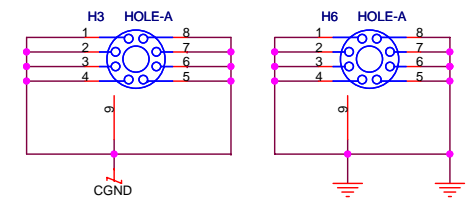
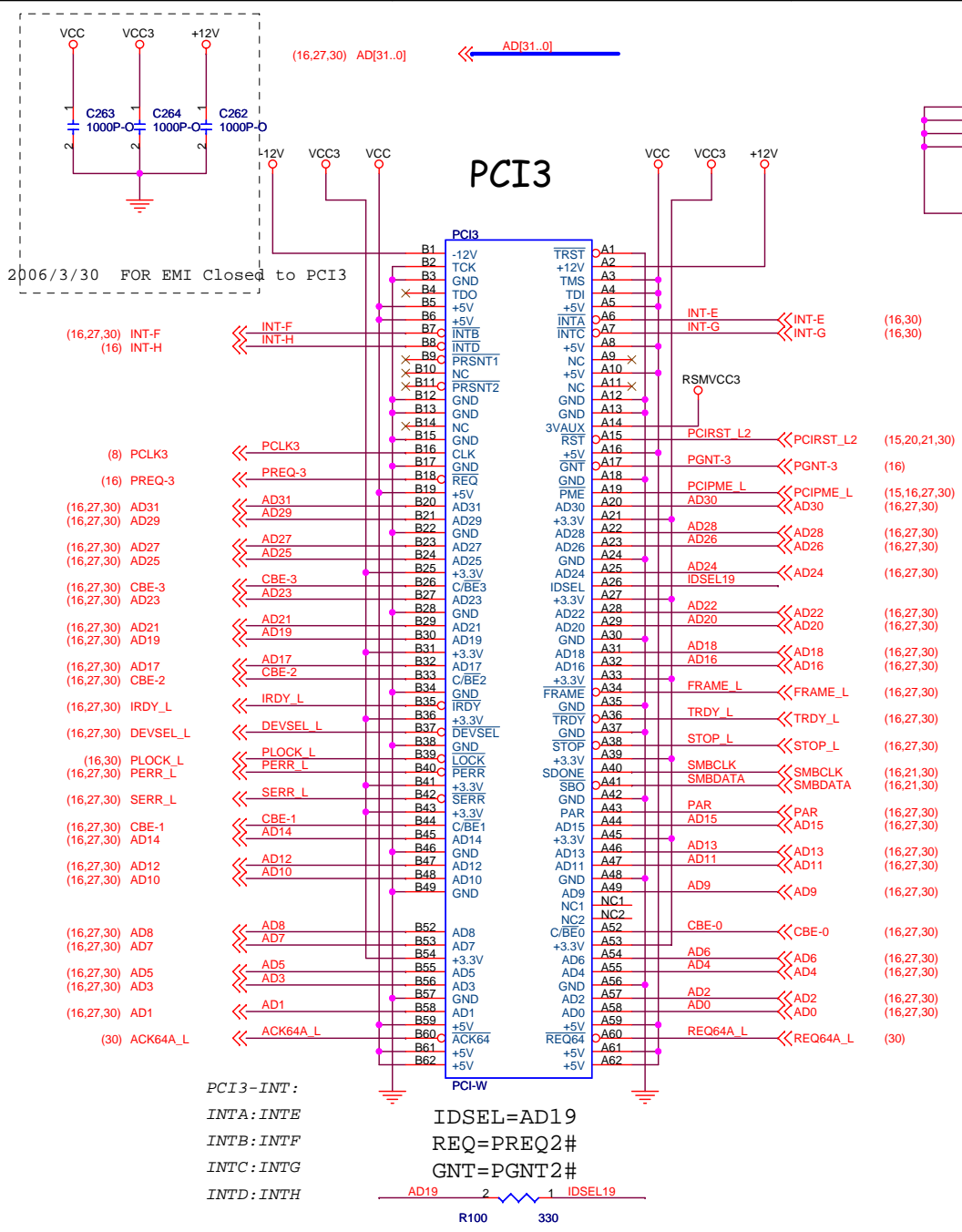


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PCI Slot 3

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Rev.C to Rev.D change for lenovo ASD overall design review issue.

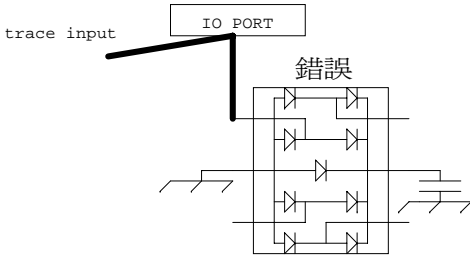
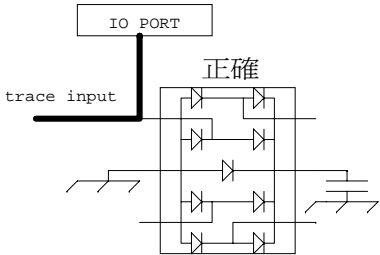
- A.Layout**
- 1.SATA1 & SATA2 differential pin pitch 太近 :try to change or modify library
 - 2.R1067 移到正面靠近CODEC1 pin
 - 3.加大 vcc power plane 於 usb3/usb4 瓶頸處
 4. CK_CPU_H / CK_CPU_L 再加長 50 mils
 - 5.CK_G_66_MCH=Y
CK_HBL_66M_ICH=Y+/- 0~0.5"
CK_G_66M_AGP=Y-(4.5~5.5")
CK_P_33M_ICH=Y+/- 0.5"
CK_P_33M_ICH 與其他CLOCK 關西錯誤需修正
 - 6.(-7705,-2095) CK_P_33M_ICH 換層處加一旁路電容C273
 - 7.(-6975,-2020) PCLK1 換層處加一旁路電容 C274
 - 8.(-6970,-1870) & (-6670,-1390) 換層處各加一旁路電容 C275,C276
 - 9.(-6950,-1785) CK_14M_AUDIO 換層處加一旁路電容C277 , 且此線太靠近島邊 (至少3H)
 - 10.(-6450,-2410) USB_48M_ICH 背面放一顆旁路電容C278
 - 11.USBP4N/USBP4P 在 (-9365,-5120)打到solder side 再走到USB3 PIN(可解決靠近島邊及vcc power plane不足問題)
 - 12.USBP7N/USBP7P 在 (-9375,-6045)打到solder side 再走到USB4 PIN(可解決靠近島邊及vcc power plane不足問題)
 - 13.5vsb 接至 u35.3 要60 mils
 - 14.移動MF1至適當位置
 - 15.Q41往下移且多打6個VIA到VCC3
 - 16.DEL RN102 ,加強Q112至 DDR2.5V電源及銅箔
 - 17.EC109,EC110 調至適當位置,CHECK PLACEMENT
 - 18.MF2.G 與 VIN 銅箔太近(有短路問題)
 - 19.(-3500,-860) LAYER2 RGB 走線 VCC 層改為GND
 - 20.ALL HUBLINK 信號 WITHIN 100 mils ,PLEASE CHECK
 - 21.PAGE 3,4 ADDED R9,R10
 - 22.PAGE 24: ADDED R17,R18,C279
 - 23.PAGE27: ADDED R21,R30
 - 24.PAGE28: DEL RN106,RN107
DEL EC40,ER81,ER80,U11,RN91,RN92
 - 25.PAGE29: ADDED R32
 - 26.PAGE 24:U34.74 改接 RTCVCC
 27. NET 'H_PWRGD' 走線間距改為 13/7/13
 - 28.NET THRMDN,CPU_THERM1 要平行走 線寬 10 mils 間距 10 mils (10/10/10/10/10)
 - 29.net AVDDL & XTALO 間距太近(拉大到20 mils)
 - 30.ER102 移到南橋背面
 - 31.N27881084,N27881347 加寬至 10~15 mil
 - 32.MC121 要靠近 U36 PIN 1
 - 33.Q41.D PIN VCC3 VIA 再加4個
 - 34.到MCH1的2_5VSTR的COPPER 加大到200 mils以上(5.7A)
 - 35.U15的第1pin DDR2_5V trace只有20mil 請增至50 mils
 - 36.VDDQ 在 BC61處多打3個VIA
 - 37.U45 下面增加 THERMAL (GROUND) PAD
 - 38.RHSYNV,YVSYC 在U32處出現直角要修正
 - 39.C61,C26;C93,C94的GROUND VIA共用一個 ,要分開打
 - 40.D49,D50,D51 供電壓改為 VDDQ
 - 41.PAGE14: ADDED R1 擴流電阻
 - 42.PAGE14:ADDED BC1
 - 43.U32 PIN 14 改接VCC
 - 44.MODIFY SATA1,SATA2 PART LIBRARY TO AVOID DIFFERENTIAL PIN SHORT
 - 45.PAGE 12 and 13 ADD termination R1073,R1074,R1075,R1076,R1077,R1078
 - 46.ADD R1072 for Giaga Lan 3.3V

B.BOM Modify

- 1.R1067 47-04 改至component side SMD BOM
- 2.ADDED R9,R10, 0 ohm 0603
- 3.ADDED R17,R18, 0 ohm 0402
- 4.ER102 改至 component side smd bom
- 5.ADDED R1, 10K ohm 0603
- 6.ADDED BC1, 0.1uF 0402
- 7.U32 CHANGE TO 74HCT32 (02-119-032132)
- 8.DEL RN91,RN92,U11,ER80,ER81,EC40
- 9.R37 CHANGE TO 4.7K ohm R0402
- 10.DEL D46,D34
- 11.DELETE EC97,EC99
- 12.ADDED RT3 10K 0603 THERMISTER
- 13.ADDED ER209,ER210,ER211,ER212
- 14.DELETE EC98,EC96
- 15.F11 零件改回原來的FUSE
- 16.ADDED BC361-BC368 0.1uF 0402 CAP
17. ADDED ER209,ER210,ER211,ER212 0 ohm 0402
- 18.ADDED R1073-R1078 100 ohm 0402

2006/07/04 MEETING


- 1.DELETE EC97,EC99 ,將VIN PLANE 拉齊
- 2.CHANGE F11 LIBRARY MOVE EC93,CHOKE4 到適當位置,MF2 下面之VIN ISLAND 往左上移,使VIN ISLAND 加大
- 3.修改R.G.B 走線,使其不跨太多電源層走線
- 4.CHECK ESD PROTECT LAYOUT COMPONENT
PLEASE CHECK U42,U43,U48,U38,U39,
D56,D58,D59,D57,D26,D27,D30,D31
D28,D29,D32,D33



- 5.PLEASE CHECK RGB 走線及 SPACING ,走線SPACING 要保持 20 MILS 以上
- 6.VGA PORT 第三層(gnd) 缺口改向左下方
- 44.CHANGE GPI6,GPI7 PULL HIGH FROM RSMVCC3 TO VCC3(INTEL ICH5 DATASHEET ISSUE)

2006/07/06 modify

1. added R1072-R1078
R1073-R1078 擺放的位置請參考PAUL 之前做的圖,如附件.
- 2.R1067 移到靠近南橋,要放在 COMPONENT SIDE
- 3.U1底下 (LAYER2) LAN 走線處改為GND,使LAN走線參考GND
4. 2_5VSTR 多打 4個VIA (-6390,-5415) AGP 下方
- 5.Q45.D 多打兩個VIA 到 2_5VSTR
- 6.USB 走線間距不對 20/7.5/7.5/7.5/20
- 8.加測試點
- 9.PAGE 28:ADDED ER209-ER212 FOR TEST POINT

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